VME-SCSI HOST ADAPTER

Hardware Reference Manual

Integrated Solutions

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Integrated Solutions
1140 Ringwood Court
San Jose, CA 95131
(408) 943-1902

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PREFACE

This manual describes the Integrated Solutions ACB-SCSI, which is used with Adaptec controllers, and the SCSI/U, which adapts the host to any device with an embedded SCSI controller. The manual is divided into the following sections:

- Section 1 provides a product overview.
- Section 2 describes specifications.
- Section 3 describes how to configure and install the VME-SCSI board.
- Section 4 describes the software interface between the ACB-SCSI and the host.
- Section 5 describes the software interface between the general purpose SCSI/U and the host.

Additional information can be found in the following publications:

American National Standard for Information Systems (ANSI)
Small Computer System Interface(SCSI) document, ANSI X3.131-1986
SCSI ANSI X3T9.2
SCSI ANSI Standard 39.131-1986
Adaptec ACB-4000 OEM Manual
NCR 5385 SCSI Protocol Controller MC-704 MC-903

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SECTION 1: INTRODUCTION

Integrated Solutions manufactures two Small Computer System Interface (SCSI) boards. In terms of hardware, both boards are identical and conform to standard SCSI interface requirements as well as to all VMEbus interface requirements. In this manual, either board is generically referred to as a VME-SCSI, when characteristics common to both boards are being described.

The difference between the boards is in their functionality which in turn is determined by the controlling firmware. The Universal Host Adapter SCSI (SCSI/U) is driven by firmware that allows the board to interface to any device with an embedded SCSI controller, including tape drives, magnetic and optical disk drives, and laser printers. The ACB-SCSI is designed to interface only with embedded Adaptec equipment; specifically, it is used only in conjunction with Adaptec 4000 ST 506; 4070 ST 506 2,7 RL; and 5580 SMD targets.

The SCSI/U is shown in relation to other major boards on a VMEbus and SCSI bus in Figure 1-1; the ACB-SCSI is shown in Figure 1-2.

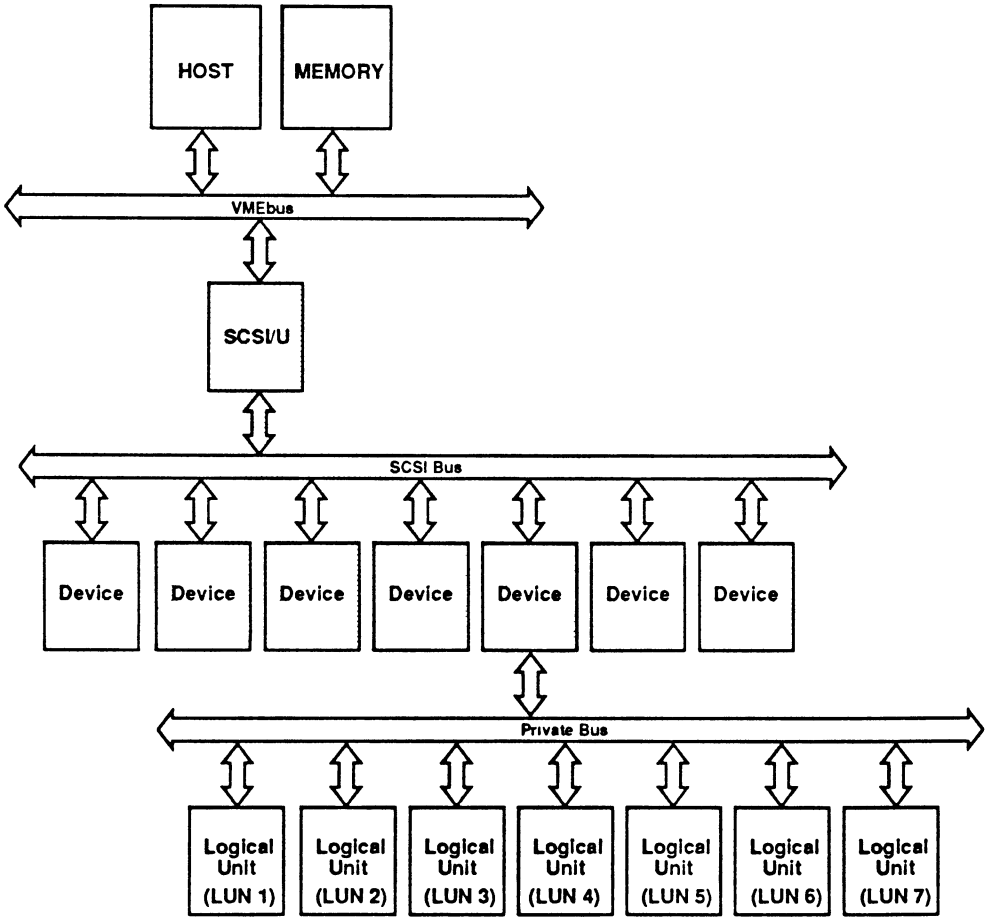

Figure 1-1. SCSI/U Implementation on a VMEbus

1.1 Hardware Design

The VME-SCSI hardware design, shown in Figure 1-3, consists of the following hardware modules:

- VMEbus interface logic
- A 16-bit control microprocessor
- A regport and an access port that allow communication over the VMEbus between the host and the SCSI control microprocessor.
- A DMA transfer port with 24 address and 16 data lines
- EPROM resident firmware
- A 16K byte RAM buffer
- A byte-word assembler/disassembler
- A SCSI Protocol Controller (SPC).

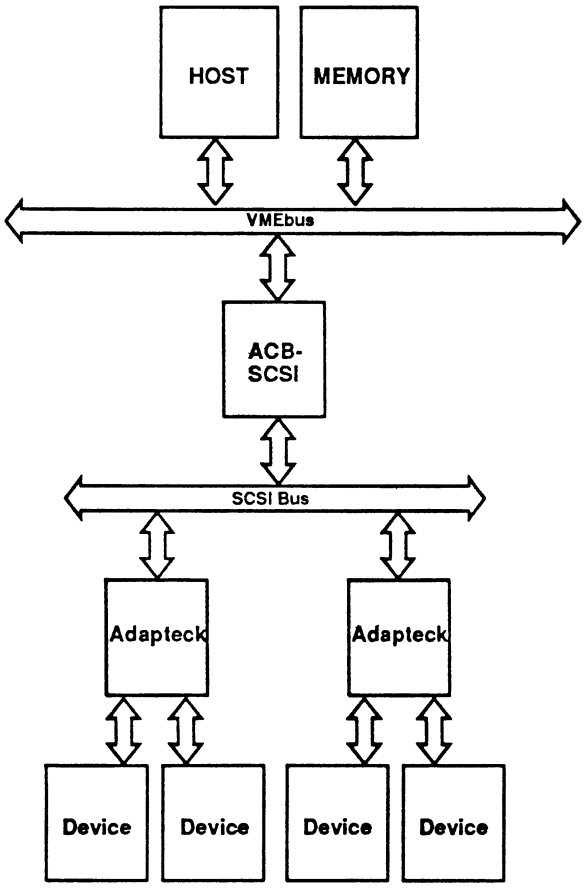

Figure 1-2. ACB-SCSI Implementation on a VMEbus

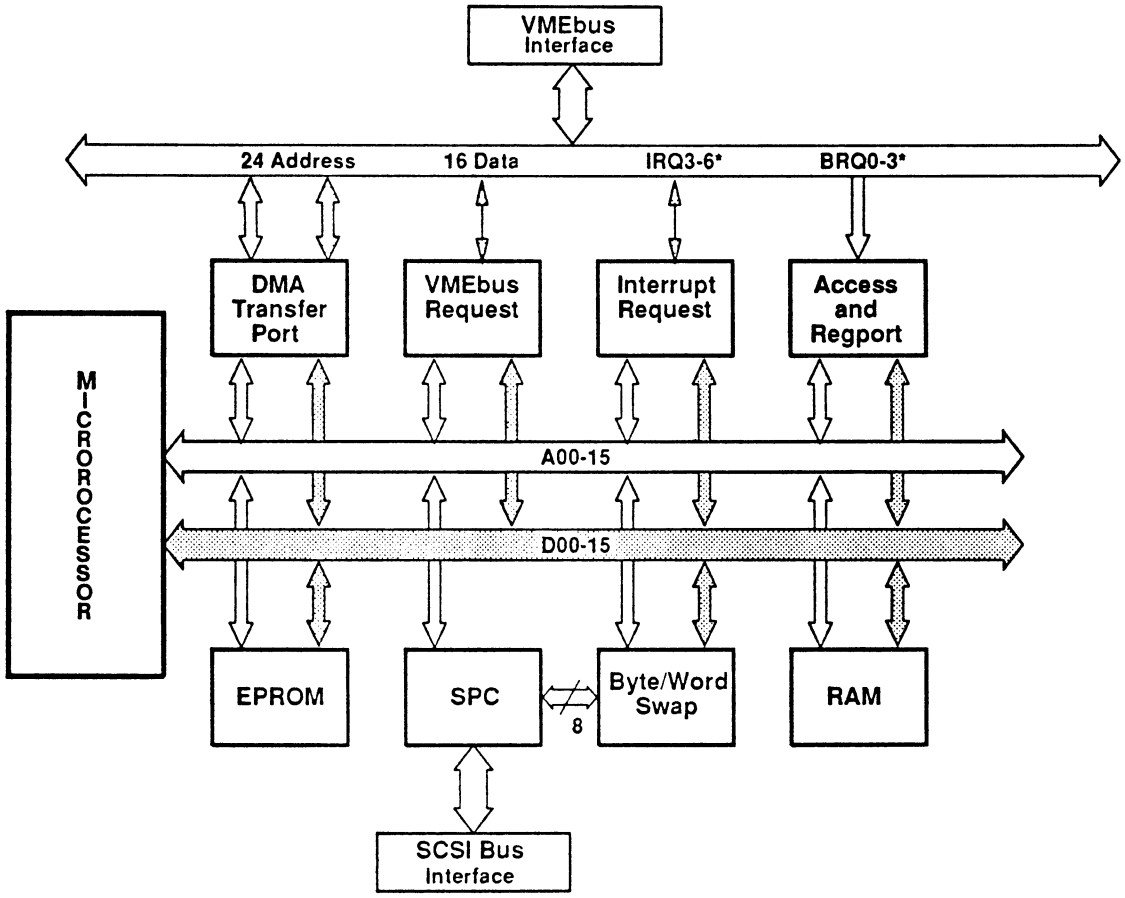

Figure 1-3. VME-SCSI Block Diagram

1.1.1 VMEbus Interface

A VME-SCSI resides in a VMEbus system card cage and is connected by a single, 96 pin connector (P1) to the VMEbus backplane. (See Section 2: Table 2-2 for P1 pin assignments.) The VMEbus interface is consistent with all applicable VMEbus logical and electrical specifications and implements a priority interrupter and bus requester as standard VMEbus functional modules.

1.1.2 Address and Data Lines

A VME-SCSI has 24 address lines on the VMEbus side and resides in standard address space. The on-board microprocessor has 16 address lines, but generates standard VMEbus addresses (A0-A23 lines) through a DMA transfer port. If the VME-SCSI broadcasts a non-existent address, a timeout error occurs on-board, and the adapter is vectored to an interrupt routine.

Data transfers occur over 16 lines to the VMEbus.

1.1.1.2 Access Ports and Virtual Registers

The access port is a CPU controlled state machine that monitors the VMEbus address lines and uses three lines (A01-A03) to identify the address of eight *virtual registers* on the VME-SCSI bus. If a register address is present on the VMEbus, the access port detects it on the falling edge of the VME address strobe and flags the microprocessor. The VMEbus registers are called *virtual* because, physically, they do not exist. The microprocessor reads VME address lines 0A1*-0A3* and VME WRITE* to determine the appropriate response. The control microprocessor then responds by reading or writing to regport.

The base VMEbus address for *virtual* registers is selected by jumpers that represent VMEbus address lines A04* and A05*. The ACB-SCSI carries on all communication with the host computer through these eight registers, including receiving commands and returning status. The SCSI/U only recognizes and responds to the base address register (r0, default FFFFD0) then obtains commands and returns status through DMA packet transfers across the VMEbus. The jumpers produce the following base address options:

FFFFC0-FFFFCE (FFFFC0 is the default for the SCSI/U)
3FFFFD0-FFFFDE (Default for ACB-SCSI)
FFFFE0-FFFFEE
FFFFF0-FFFFFE

Access port and regport are not VMEbus functional modules, although they conform to all addressing specifications for slave modules on the VMEbus.

1.1.1.3 Bus Requester

The bus requester module implements Bus Request/Bus Grant protocol at all four VMEbus levels, including request propagation at levels other than its own (BG0IN*-BG3IN*, and BG0OUT*-BG3OUT*) through a daisy chain to multiple requesters on the bus. The open collector, bus request signal level (BR0*-BR3*) is selected on board by jumpers and is therefore static (STAT) and can not be changed dynamically by the software.

The SCSI/U normally requests the bus periodically for DMA transfers of its control register or for exchanging command and status packets with the host. It also requests the bus to service SPC commands for DMA data transfers, as does the ACB-SCSI.

1.1.1.4 Master and Slave Modes

The VME-SCSI is capable of acting either as bus master or slave depending on the requirements of its particular task. Either SCSI is bus master when it initiates DMA data transfers, and the SCSI/U must also obtain the bus to read its control register and fetch command packets from, or return status to, host memory. A VME-SCSI operates either as a Release When Done (RWD) or Release on Request (ROR) bus master.

When in bus master mode, the bus time out (TOUT) is 8 µs.

If the host asserts a BCLR* signal, the VME-SCSI produces a non-vectored interrupt (NVI) on board which releases the VMEbus, after which the SCSI immediately arbitrates for it again.

A VME-SCSI normally operates in slave mode immediately after it is initialized or when it is waiting for a bus master to address a target in preparation for data transfers.

The interface sequences for bus requester and master and slave modes are tightly interlocked through firmware to the microprocessor wait signal which remains asserted until the bus grant signal has occurred. The slave read and write cycles interlock through the firmware to delay the VMEbus DTACK signal until the proper internal signal sequence occurs.

1.1.1.5 Interrupter Module

An interrupt cycle is initiated when the firmware asserts its interrupt request signal. The cycle is completed in hardware.

When an interrupt is pending, the interrupter module asserts the interrupt request line (IRQ3*-IRQ6*), waits for IACKIN*, detains IACKOUT*, and supplies an interrupt vector (Status/ID) when it has been acknowledged. A VME-SCSI allows optional selection of interrupt levels 3-6 and is strapped at one of the optional levels by on-board jumpers. The level is therefore statically set (STAT) and can not be dynamically changed by software. The factory default setting is 6. (See Section 3 for the number and location of all interrupt related jumpers.) The interrupt vector is also jumper selectable from eight on-board options listed in the following:

60_H
64_H
68_H
$6C_H$
70_H
74_H
78_H (Default)
$7C_H$

If the interrupter module is not at the interrupt level being serviced, or if it has no pending interrupts on board, it simply propagates the IACKIN*/IACKOUT* bus signals down any of the seven levels of the VMEbus interrupt daisy chain.

For more detailed information on VMEbus interrupter modules, refer to the *VMEbus Specification Manual*, Rev. C.1, HB212.

1.1.2 EPROM

The firmware that controls and monitors all VME-SCSI operations resides in two 2732-2 EPROMs, one containing the high- and one the low-order nibble of a command byte. The SCSI/U firmware supports any application that requires driving a device with an embedded SCSI controller. The Adaptec firmware supports either the ACB-4000 or the ACB-4070 or the ACB-5580 embedded controllers.

All EPROMs are installed in sockets to facilitate field upgrades.

1.1.3 Control Microprocessor

The high-speed 16-bit microprocessor operating at 8MHz is completely under firmware control. In turn, it monitors or controls all communications across the VMEbus through the on-board bus request module, the interrupt request module, the access port, and regport. Controlling VMEbus access includes performing DMA transfers across the bus.

The control microprocessor is also an interrupt driven, real time monitor that initializes all commands for data transfers, then monitors them through interrupts from the SPC. Interrupts to the microprocessor call vectored service routines. Routines that inform the host of transfer progress include status reporting (either completions or errors) and a service for pending messages.

The microprocessor also maintains the current and saved pointers required for servicing disconnect and reconnect requests from SCSI devices.

Use of a 16-bit microprocessor gives the VME-SCSI a high level of functionality to carry on data transfers to peripheral devices, including access to host memory, without host intervention.

1.1.4 SCSI Protocol Controller (SPC)

The on-board SPC is an NCR 5385E or 5386 asynchronous interface chip that transfers data to and from targets using SCSI protocol. Data transfers are 8 bits wide, with one additional bit for parity. The SPC also has nine dedicated control lines.

Command sequences begin when the firmware sends a select target command to the SPC, which independently establishes the SCSI interface. The SPC then interrupts the microprocessor when phase

changes occur, when DMA transfers are required across the VMEbus, or when the command is completed. If errors are encountered, the SPC interrupts the microprocessor for recovery processing. Timing loops and microprocessor wait states established in firmware interlock the SPC interrupts to other, on-board microprocessor functions under firmware control.

For more detailed information on the SPC, refer to the NCR specifications in *NCR 5385E/5386 SCSI Protocol Controller User's Guide* MX-903 5/85.

1.1.5 RAM Buffer

VME-SCSI boards have a 16K byte RAM that buffers data transfers between an initiator and target and also provides approximately 2K of on-board RAM for data structures used by the firmware. In the SCSI/U, all data transferred between target devices and host memory are buffered in the on-board RAM. Segmentation of the buffer is set by the firmware, and will vary with the firmware version.

The ACB-SCSI also uses some on-board RAM for main memory that retains updated virtual registers and the like. The RAM used for data transfer buffers is segmented into 2K, 4K, or 8K segments by firmware and can not be dynamically reallocated.

1.1.6 Byte-Word Assembler/Disassembler

The SPC data bus is 8 bits wide, with one additional parity bit. To allow full 16 bit wide transfers across the VMEbus and over the internal VME-SCSI bus, a byte swap buffer is provided in hardware that takes two bytes of data from the internal bus and disassembles them into two 8-bit bytes for the SPC. The bytes are stored in reverse order of significance on the target media, that is, most significant byte last. Since the order is again reversed when data is retrieved, data words are removed from and replaced in host memory in the correct order. If the reverse storage order is not anticipated by some device that accesses a VME-SCSI target, which might happen by moving a disk drive to a different SCSI host adapter, provision should be made to correct the storage order in the device driver.

1.2 SCSI Bus Characteristics

VME-SCSIs are connected to the SCSI bus through connector J1, which has 8 data, one data parity, and nine command lines. (See Section 2, Table 2-2 for J1 connector pin assignments.) The SCSI bus interface supports communication between the VME-SCSI and attached peripheral devices. The following bus interface features are supported:

- Priority or round robin arbitration of bus contention (0-7).
- Multiple peripheral devices and device types.
- Asynchronous data transfer at up to 1.5 Mbytes/second.

When two or more targets are in contention for the SCSI bus, arbitration is resolved on a priority basis. In priority arbitration, the device with the highest SCSI bus ID, or address, that is requesting the bus wins the bus. Level 7 is the highest priority level and is usually assigned to the VME-SCSI adapter. If two SCSI/Us reside on a single bus, either can be assigned any priority level from 0-7.

The SCSI/U supports any device with an embedded SCSI controller and implements disconnection and reconnection, but not command chaining. The ACB-SCSI implementation does not support multiple device types, in the sense that the SCSI/U does. Rather, it is dedicated to Adaptec controllers. Neither does it support disconnection and reconnection nor command chaining.

For further details on this interface, refer to the SCSI bus specification in the *ANSI 3X.131-1986* standards manual.

1.3 LED and Diagnostics

A diagnostic LED on VME-SCSI boards provide diagnostic code during power up, to indicate the diagnostics have begun. If the diagnostics fail, the LEDs blink with long and short, encoded pulses.

On the SCSI/U the LED emits one long and two short blinks to indicate the diagnostics have begun running, and one long and two short blinks when they are completed. Failure codes are presented in Table 1-1.

Table 1-1. SCSI/U Power Up Diagnostic Codes

LED	Interpretation
One long blink	SPC diagnostics failed
Two long blinks	RAM test failed
Three long blinks	SPC interrupt failed to occur
Four long blinks	SPC did not post its function complete
Five long blinks	No SPC data full bit received
Six long blinks	Register data did not compare

A diagnostic LED on the ACB-SCSI board also provides a diagnostic aid, but the coding is different from the SCSI/U coding. At initial power-up, the ACB-SCSI LED blinks 16 times (about 30 seconds) allowing all disks to come up to speed. If a power up failure occurs, the LED blinks the codes presented in Table 1-2.

Table 1-2. ACB-SCSI Power Up Diagnostic Codes

LED				Interpretation
short	short	short	long	Could not restore the drive
short	short	long	short	Drive not ready
short	short	long	long	Seek never completed
short	long	short	short	Cannot find drive 0 on power-up
short	long	short	long	Write fault
short	long	long	short	Drive not connected
short	long	long	long	SPC phase change or self test error
long	short	short	short	SCSI target selection failed
long	short	short	long	Target controller error

1.4 Related Documents

Adaptec ACB-4000 OEM Manual
NCR 5385 SCSI Protocol Controller MC-704 MC-903
SCSI ANSI X3T9.2 ANSI
SCSI ANSI Standard 39.131-1986

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SECTION 2: SPECIFICATIONS

This section contains specifications and operating requirements for both versions of the VME-SCSI.

2.1 Form Factor

The form factor is a standard, double wide VMEbus card (160mm by 233.33mm).

2.2 Compatibility

A VME-SCSI is compatible with both VMEbus and SCSI bus electrical and logical specifications.

2.2.1 VMEbus

A VME-SCSI interfaces with the VMEbus in accordance with the electrical and logical specifications defined in the *VMEbus Specification Manual*, Motorola part number HB212, Rev C.1.

The following list shows legitimate options that are either designed into a VME-SCSI or are selected by on-board jumpers.

Data Transfer Bus	A00-A23, D00-D15
REQUESTER	The REQUESTER is jumper selectable from BRQ0*-BRQ3*
	The firmware sets this as RWD rather than ROR. It is not user-programmable.
	Bus master time out (TOUT) = 8 µs.
INTERRUPTER	IRQ3*-IRQ6* set by jumper and therefore static (STAT)
Interrupt Vector	Jumper selected from the following values: 60_H 64_H 68_H $6C_H$ 70_H 74_H 78_H (Default) $7C_H$

Table 2-1 shows the pin assignments and signal mnemonics for P1, the 96 pin VMEbus connector.

2.2.2 SCSI Bus Interface

The VME-SCSI connects to the SCSI bus through the 50 pin port connector J1. The interface conforms to all electrical and logical specifications for the bus as defined in the *ANSI X3.131-1986* standards manual.

Address	None
Control	Nine standard SCSI control lines
Data lines	Eight lines (D00-07)+ parity
Target arbitration	Arbitration for the SCSI bus is granted on a priority basis on the ACB-SCSI, within levels 0-7. Level 7, the highest level, is the default for the ACB-SCSI adapter. The SCSI bus address and arbitration level sets the SCSI/U ID, which can be any level, since it operates on a round robin priority basis. The ID is also returned if the SCSI/U is read after power up, but before a hard initialize.
Termination	Termination resistors must be installed on either end of the SCSI bus. Termination on the VME-SCSI is set by a jumper.

VME-SCSI	The SPC SCSI bus ID is hard wired by jumpers.

Pin assignments for J1 are shown in Table 2-2.

2.3 I/O Register Addresses

The host processor, and any other attached bus masters, access the VME-SCSI through eight memory-mapped I/O registers. The address of the registers is selected from among the following:
FFFFC0-FFFFCE (FFFFC0 is the default for the SCSI/U)
3FFFFD0-FFFFDE (Default for ACB-SCSI)
FFFFE0-FFFFEE
FFFFF0-FFFFFE

2.4 Target Controllers

Adaptec's ACB-4000 or ACB-4070 hard disk controller board interfaces ST506-type Winchester disk drives to the VME-SCSI host adapter as defined in Adaptec's *ACB-4000 Series User's Manual.* The ACB-4000, which controls two ST-506/412 or equivalent Winchester drives, supports standard SCSI features as well as extensions and uses MFM encoding. The ACB-4070 interfaces to ST 506/412 or equivalent Winchester drives, but uses 2,7 run length limited (RLL) encoding. The ACB-5580 SMD target is also controlled by the ACB-SCSI.

The SCSI/U controls any device with an embedded SCSI controller. For logical interface characteristics, including commands and status or sense reporting, see the manual for individual targets.

2.5 Transfer Rate

The maximum transfer rate from the target to host memory across the VMEbus is approximately 1.5 Mbytes per second.

2.6 Diagnostic Indicator

An LED located on all VME-SCSI boards indicates power on, diagnostics initiated, and error codes.

2.7 Power Requirements

The VME-SCSI power requirements are +5V @ 3.1 amps.

2.8 Environmental

The VME-SCSI environmental requirements are:

Temperature	0 degrees centigrade to 50 degrees centigrade (operating). -40 degrees centigrade to 65 degrees centigrade (non-operating).
Humidity	10 to 90 percent (non-condensing)

Table 2-1. Connector P1 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK†	BG3IN*	SYSFAIL*†
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0†	A22
17	GND	AM1†	A21
18	AS*	AM2†	A20
19	GND	AM3†	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK†	A17
22	IACKOUT*	SERDAT†	A16
23	AM4	GND	A15
24	A07	IRQ7*†	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*†	A09
30	A01	IRQ1*†	A08
31	-12V†	+5V STDBY†	+12V†
32	+5V	+5V	+5V

NOTE:

In all tables in this manual, an asterisk (*) following a signal name indicates the signal is asserted low.

† Indicates a standard VMEbus signal or power trace, but no connection is made on a VME-SCSI board.

Table 2-2. Connector J1 Pin Assignments

Pin Number	Signal Mnemonic	Signal Name
2	-DB(0)	Data Bus 0
4	-DB(1)	Data Bus 1
6	-DB(2)	Data Bus 2
8	-DB(3)	Data Bus 3
10	-DB(4)	Data Bus 4
12	-DB(5)	Data Bus 5
14	-DB(6)	Data Bus 6
16	-DB(7)	Data Bus 7
18	-DB(P)	Data Bus Parity
20	GROUND	Ground
22	GROUND	Ground
24	GROUND	Ground
26	†TERMPWR	Terminator Power
28	GROUND	Ground
30	GROUND	Ground
32	-ATN	Attention
34	GROUND	Ground
36	-BSY	Busy
38	-ACK	Acknowledge
40	-RST	Reset
42	-MSG	Message
44	-SEL	Select
46	-C/D	Control/Data
48	-REQ	Request
50	-I/O	Input/Output

† This pin is reserved for providing additional power (+5V).

SECTION 3: CONFIGURATION

This section describes how to configure a VME-SCSI board. Figure 3-1 shows jumper and switch locations on the board. Jumpers set configuration options for both the VMEbus and SCSI bus interfaces. Factory defaults are indicated in **boldface** in the text and as installed jumpers on Figure 3-1.

3.1 VME Interface Jumpers

VMEbus interface jumpers consist of the following:

- VMEbus Address for Regport
- Bus Request
- Interrupt Request
- Interrupt Vector

3.1.1 VMEbus Address

Jumper settings E18 through E21 map regport on the VME-SCSI into one of four VMEbus address locations. (See Table 3-1.) The jumpers represent VME address bits A04* and A05*. The factory default sets jumpers E18 and E21.

Table 3-1. VMEbus Address Jumpers

Address	A 5	A 4	E18	E19	E20	E21
FFFFC0-FFFFCE	0	0	jmpr	open	jmpr	open
FFFFD0-FFFFDE	**0**	**1**	**jmpr**	**open**	**open**	**jmpr**
FFFFE0-FFFFEE	1	0	open	jmpr	jmpr	open
FFFFF0-FFFFFE	1	1	open	jmpr	open	jmpr

3.1.2 Bus Request

Jumpers E44-E55 set the bus grant in and out lines BG0IN*-BG3IN* and BG0OUT*-BG3OUT*. Jumpers E36-E39 set the bus request level BRQ0*-BRQ3*. Set all the jumpers as shown in Table 3-2 so the in, out, and request lines will be at the same level for the entire board. The factory default is BRQ3 (BRQ3).

Table 3-2. Bus Request/Grant Jumpers

Bus Request Level	Jumpers
0	E36, E44, E46, E48, E51, E54
1	E37, E45, E47, E49, E51, E54
2	E38, E45, E48, E50, E52, E54
3	**E39, E45, E48, E51, E53, E55**

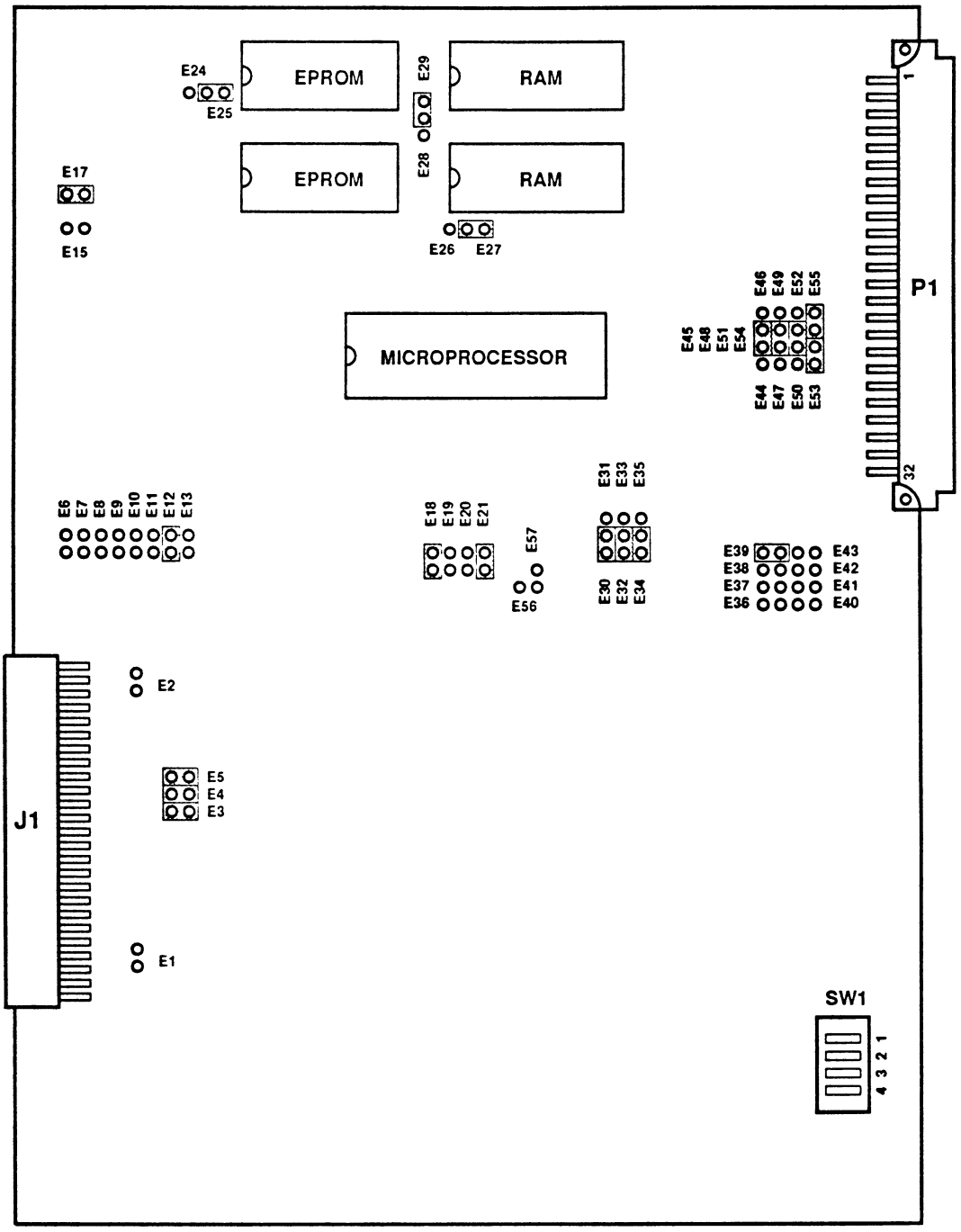

Figure 3-1. VME-SCSI Board Layout

3.1.3 Interrupt Request

Switch settings 1-3 on SW1 set the board level for interrupt requests. Table 3-3 represents the Interrupt Request (IRQ) switch settings. The factory default is level IRQ6.

Table 3-3. Interrupt Request Switch Settings

Interrupt Request Line	Bit 1	Bit 2	Bit 3
3	open	open	closed
4	closed	closed	open
5	open	closed	open
6	**closed**	**open**	**open**

3.1.4 Interrupt Vector

Jumpers E30-E35 set the interrupt vector address at a value between 60_H to $7C_H$, as Table 3-4 shows.

Table 3-4. Interrupt Vector Jumper Configurations

Vector #(h)	E30	E31	E32	E33	E34	E35
60	open	jmpr	open	jmpr	open	jmpr
64	open	jmpr	open	jmpr	jmpr	open
68	open	jmpr	jmpr	open	open	jmpr
6C	open	jmpr	jmpr	open	jmpr	open
70	jmpr	open	open	jmpr	open	jmpr
74	jmpr	open	open	jmpr	jmpr	open
78	**jmpr**	**open**	**jmpr**	**open**	**open**	**jmpr**
7C	jmpr	open	jmpr	open	jmpr	open

3.2 SCSI Interface Jumpers

Jumpers configure the following SCSI interface characteristics:

- SPC ID
- SCSI Arbitration ID
- SCSI Termination
- RAM Configuration

3.2.1 SPC ID0*-ID2*

Three input signals to the SPC encode its SCSI bus identification number. This number allows the controller to know when it is being addressed over the SCSI bus, and to let a target return an acknowledgement. A SCSI/U returns this identification in the low order byte of IDENT. Table 3-5 specifies the correct jumper configuration for each bus ID. The factory default is Bus ID 7. After the VME-SCSI arbitrates for and wins the SCSI bus, it asserts its ID on the bus through jumpers to odd numbered pins 2-16 on connector J1. The target on the bus knows which initiator is addressing it by the J1 pin identification. It is essential, therefore that the VME-SCSI ID set with jumpers E3-E5 match the bus ID pins set by E6-E13. Table 3-6 shows the relation of E6-E13 to the SCSI bus ID slots 0-7.

Table 3-5. SPC ID Jumpers

Bus ID	E5	E4	E3
0	open	open	open
1	open	open	jmpr
2	open	jmpr	open
3	open	jmpr	jmpr
4	jmpr	open	open
5	jmpr	open	jmpr
6	jmpr	jmpr	open
7 (Default)	**jmpr**	**jmpr**	**jmpr**

3.2.2 VME-SCSI Arbitration ID

Each target and initiator (usually the SPC) on a SCSI bus has a unique arbitration ID that it asserts after gaining the SCSI bus. The purpose of the ID is to let a selected target know the identification of the initiator after arbitration. The jumper selection for this ID must match the SPC ID setting selected with jumpers E3-E5.

Table 3-6. SCSI Arbitration Level

Arbitration Level	Jumper Position
0	E06
1	E07
2	E08
3	E09
4	E10
5	E11
6	E12
7(Default)	**E13**

3.2.3 SCSI Termination

When a VME-SCSI board is positioned at either end of the SCSI bus, it must be terminated by having jumpers installed on E1 and E2.

3.3 Miscellaneous Jumpers

Jumpers that are not related to a bus interface also exist on the VME-SCSI. These include the RAM size option, the EPROM size option, and a parity enable jumper. The ACB-SCSI also has a jumper selection to indicate which Adaptec drive is on the bus. A format enable option is set by SW1 switch and is used only on ACB-SCSI boards. Jumpers installed on E57 and E57 divide the on-board oscillator frequency, but are not changeable in the field.

3.3.1 RAM

Two internal RAM buffer sizes are available on the VME-SCSI board, 2K x 8 or 8K x 8 static RAMs. Using Table 3-5, configure jumpers E26, E27, E28, and E29 according to the size of RAM included on your board

Table 3-7. RAM Jumper Configurations

Jumper Number	2K x 8	8K x 8
E26	jmpr	**open**
E27	open	**jmpr**
E28	jmpr	**open**
E29	open	**jmpr**

If the VME-SCSI board is configured with the 2K buffer option, install a jumper at E17.

3.3.2 EPROMs

ISI always supplies 2732 EPROMs, so the E24-25 jumpers are always installed on E25. (If for some reason, your board has 2716 EPROMs, the jumpers are always installed on E24.)

3.3.3 Disk Format Enable (SW1)

SW1 is a four-pole switch that has been described in conjunction with the first three switches (1-3) that set the interrupt request level. The fourth pole sets the Disk Format Enable functions when the board is used with Adaptec ACB-4XXX and ACB-5580 boards. To enable the format option set SW1-4 on.

3.3.4 Microprocessor Crystal Setting

The crystal frequency used for timing cycles in the microprocessor can be divided by 2 with jumper E56 installed or divided by 4 with E57 installed. The placement of these jumpers is dependent on the factory installed oscillator. The jumpers should not be changed in the field.

3.3.5 Adaptec ID Jumpers

On the ACB-SCSI jumpers E15 and E17 are set at the factory. E17 should always be installed. E15 should be installed with the Adaptec ACB-4000, but removed with the Adaptec ACB-4070.

3.3.6 SCSI/U Parity

On the SCSI/U board, jumper E15 is installed to enable parity. Parity checks are disabled if E15 is open. E17 is not used on the SCSI/U.

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SECTION 4: ACB-SCSI SOFTWARE INTERFACE

This section describes the software interface between a host and the ACB-SCSI host adapter. The interface is implemented at two ports, the access port and regport. The ACB-SCSI responds to a host access at regport after power up and after the ACB-SCSI has run self-diagnostics.

4.1 Initialization

Immediately after power up, but before the ACB-SCSI begins diagnostics, it sets the Controller Busy (CB) bit in its command register which is r 0— the base VMEbus address set by on board jumpers. Any attempt to access the SCSI while it is busy with diagnostics will result in a return which indicates the SCSI is present, but busy. The ACB-SCSI sets its CB bit whenever it is not monitoring access port and waiting for the host to access regport.

Diagnostics consist of checking the SPC and then writing and reading each target on the SCSI bus to determine whether it has good status after power up. The SCSI then clears the command bits in r0, resets the CB bit, and begins monitoring access port for host accesses. The following errors are fatal during power up, but are reported in the Control Status Register at other times:

1	The disk would not home in maxcyl+1 steps.
2	The disk never became ready or tried and returned to not ready.
3	The seek did not complete in maximum seek time.
4	Can not find drive 1 on power up.
5	Power up failure.
6	A write fault was detected.
7	No drives were found during power up.
8	A phase change error, or SCSI Protocol Controller (SPC) error, or vectored interrupt error occurred.
9	An attempt to select a target failed.
10	A SCSI class 01 SENSE byte error, including target controller errors not otherwise specified.
11	A SCSI class 02 Sense byte error, which includes an improperly specified control parameter. This code also indicates the host issued a non-implemented instruction.

4.2 Access Port

If the diagnostics are successful, the ACB-SCSI resets its CB bit and begins monitoring access port. When the host accesses any one of the eight addressable registers in regport, the access port recognizes the register's address on the leading edge of the address signal, and the ACB-SCSI strobes it into RAM on the falling edge. The register names and addresses are listed in Table 4-1, where "x" is jumper selectable for the Hex values C, D, E, or F. Byte access to these registers is not supported.

4.3 Regport

The eight addressable, 16-bit registers in regport allow the SCSI and host to exchange control, command, and status information across the VMEbus. The host addresses each register as a separate VMEbus location. If the ACB-SCSI is ready to accept a regport access, it will have set its controller busy bit (CB) off. If it is *busy* the CB is set on, and data cannot be transferred to or from the registers, although the ACB-SCSI generates a return to complete the access cycle.

Table 4-1. Register Addresses

VMEbus Address	Register Name
$FFFFx0_H$	Control/Status Register
$FFFFx2_H$	Disk Address Register
$FFFFx4_H$	Bus Address Register
$FFFFx6_H$	Word Count Register
$FFFFx8_H$	Address Extension Register
$FFFFxA_H$	Sense Word Register 0
$FFFFxC_H$	Sense Word Register 1
$FFFFxE_H$	Sense Word Register 2

This high-level host interface protocol permits a simple sequence of operations for software drivers that load the ACB-SCSI command and parameter registers in regport. The four steps required are listed below. The first three steps can be completed in any order.

1. The Disk Address Register and Address Extension Register must contain the first logical block number to be read or written.
2. The Bus Address Register and Address Extension Register must contain the beginning address in system memory to be read or written.
3. The Word Count Register must contain the number of words to be transferred.
4. The final operation is to write the Control/Status Register with the command to be executed.

4.3.1 Control Status Register (CSR)

The Control Status Register (CSR) is a 16-bit word addressable register. Bits 1 through 9 can be read or written; the other bits can only be read. Figure 4-1 shows the CSR format. A description of the function of each bit follows the figure.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CE	DB	Error Field				DS	DS	CB	IE	Not Used		CMD Field			Not Used

Figure 4-1. Control Status Register Format

When the controller is initialized, or immediately after power up, bits 1-6 and 8-13 are cleared and bit 7 is set.

CSR Bit Definitions:

Bit 0	Not used.	
Bits 3-1	Command Field	The specific command to be executed by the target device is specified in this field. See subsection 4.5 for individual commands.
Bits 4-5	Not used.	
Bit 6	Interrupt Enable	This bit instructs the ACB-SCSI to interrupt the host after normal command completion or completion with an error. The ACB-SCSI initiates communication with the host by issuing a host interrupt request with one of eight jumper-selectable interrupt vector addresses: 60h, 64h, 68h, 6Ch, 70h, 74h, 78h (factory default), or 7Ch. Instructions for setting the interrupt vector are given in Section 3. If the interrupt enable bit is not set, the host polls the CSR for command completion.
Bit 7	Controller Busy	When the controller clears this bit it indicates to the host that it is ready to accept a command. When set by the host, this bit indicates to the controller that a command to be executed has been set in bits 3-1. The ACB-SCSI also sets this bit when an error occurs.
Bits 9-8	Drive Select	The host sets this field to specify one of four possible target devices for which a command is intended.
Bits 13-10	Error Field	Each bit in this field represent a specific error. If more than one bit is set, multiple errors have occurred. Any combination of bits may be set, but each still represents the same error, whether it occurs alone or in combination.
Bit 10	Operation Incomplete	The command terminated prior to completion.
Bit 11	SCSI Target Check	An error has been detected by the target controller. Specific details relating to that error are available in Sense Words 0-2.
Bit 12	Host Adapter Check	An error has been detected by the ACB-SCSI. The SCSI command that was active at the time of failure and the corresponding error code is available in Sense Word 0.
Bit 13	Non-Existent Memory	The ACB-SCSI has attempted to reference a location in host memory from which there has been no response.
Bit 14	Device Busy	This bit is set by the host adapter whenever the host CPU attempts to select a target device that is busy, e.g., a disk with a seek in progress.
Bit 15	Composite Error	This bit is set by the ACB-SCSI to indicate one or more of the bits in the error field (bits 13-10) has been set. If the Interrupt Enable bit (Bit 6) has been set and an error occurs (which also sets bit 7), an interrupt is generated.

In addition to the CSR, the host normally writes four more regport registers when sending a command to the ACB-SCSI. These registers are the Disk Address Register (DAR), the Bus Address Register (BAR), the Word Count Register (WCR), and the Address Extension Register (AER). Each of these registers is 16 bits wide. The host can read or write each of them.

4.3.2 Disk Address Register (DAR)

The DAR is cleared either by initializing the ACB-SCSI or by loading the register with zeros. It contains the two low order bytes of an address pointer to logical blocks on disk when the command is a Read or Write Data command. It contains formatting information when a Format command is being executed. The

different formats are shown in the Read Data, Write Data, and Format command descriptions. (See subsections 4.5.4 and 4.5.5.)

4.3.3 Bus Address Register (BAR)

The BAR is a pointer to the two, low-order, address bytes of the first location in host memory which data is to be transferred to or from when the Read or Write Data command is issued.

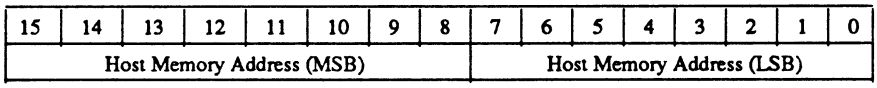

Figure 4-2. Bus Address Register Format

4.3.4 Word Count Register (WCR)

The WCR specifies the total number of words to be transferred to or from VME host memory during data transfer operations.

If a data transfer operation does not proceed to completion, this register contains a residual count indicating the number of words that failed to transfer to or from host memory.

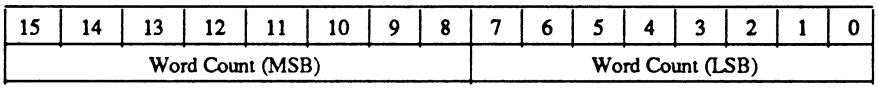

Figure 4-3. Word Count Register Format

4.3.5 Address Extension Register (AER)

The AER contains the high-order byte of the first location in host memory to or from which data is to be transferred in its LSByte. It also contains the high-order byte of the first logical block address on the target to or from which data is to be transferred.

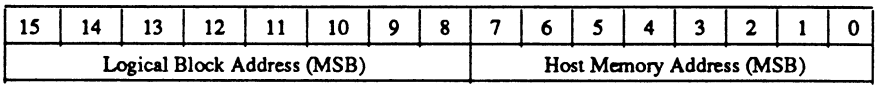

Figure 4-4. Address Extension Register Format

4.4 Command Descriptions

The following paragraphs describe the commands supported by the ACB-SCSI, specify the associated parameters, and describe command completion results that can be expected following command execution.

Table 4-2. Command Codes in CSR

Bit 3	Bit 2	Bit 1	Definition
0	0	0	Format
0	0	1	N/A *
0	1	0	Size
0	1	1	Seek
1	0	0	N/A
1	0	1	Write Data
1	1	0	Read Data
1	1	1	N/A

* Not assigned

4.5 Host Adapter Commands

Certain commands are directed to the ACB-SCSI board itself, which is a target on the SCSI bus, just as the target devices are. Commands specific to the adapter board are shown in Table 1-3.

Table 4-3. Host Adapter Commands

Operation Code	Description
$F0_H$	Follow-up command to acquire 8 more bytes of immediate data. A host adapter code of 82_H will indicate when this command should be used.
FB_H	Set-up host adapter operational parameters. This command has some data associated with it as follows: byte 0 = (default) byte 1 = (default)
FE_H	Read host adapter firmware level
FF_H	Reset SCSI bus

4.5.1 Seek Command

The seek command (CSR bits 3-1, Op Code 100) positions the addressed drive at the logical block specified. The logical block address must also be specified for reads and writes following a seek. When a seek command is completed, the SCSI sets controller ready and drive ready status bits. If the IE bit was set a host interrupt is activated.

4.5.2 Size Command

The size command (CSR bits 3-1, Op Code 010) returns the formatted geometry of the specified disk drive in the following registers:

1. DAR provides the number of heads
2. BAR provides the block size
3. WCR provides the number of sectors per track
4. AER provides the number of formatted cylinders

When a size command is completed, the SCSI sets controller ready and drive ready status bits. If the IE was set, a host interrupt is activated.

4.5.3 Write Data Command

The write data command (CSR bits 3-1, Op Code 101) transfers data from host memory to the addressed target. Parameters related to the transfer are specified in the following registers.

1. DAR—The address of the first logical block to which data is written on the target is specified in the DAR and the MSB of the AER.
2. BAR—The address in host memory from which the transferred data is fetched is specified in the BAR and the LSB of the AER.
3. WCR—The total number of words to be transferred is specified in the WCR.

When Write Data is completed, the SCSI sets controller ready and drive ready status bits. If the IE bit was set in the CSR, a host interrupt is activated.

If the transfer failed to complete successfully, error status bits are set. If appropriate, information relating to the failure is stored in the SCSI sense word registers.

4.5.4 Read Data Command

The read data command (CSR bits 3-1, Op Code 110) transfers data from the target to host memory. Parameters related to the transfer are specified in regport prior to writing the command to the CSR.

1. DAR—The address of the first logical block from which data is to be read on the target is specified in the DAR and the MSB of the AER.
2. BAR—The address in host memory to which the data is to be transferred is specified in the BAR and the LSB of the AER.
3. WCR—The total number of words to be transferred is specified in the WCR.

When Read Data is completed, the SCSI sets controller ready and drive ready status bits. If the IE bit was set, the host is interrupted.

If the transfer failed to complete successfully, error bits are set and appropriate information relating to the failure is stored in the SCSI sense word registers.

During a read, write, or seek command, the DAR is loaded with the two low-order bytes of the address of the first logical block to be transferred (see Figure 4-5). This register is not updated with successive block transfers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Logical Block Address (MSB)								Logical Block Address (LSB)							

Figure 4-5. DAR During Read/Write/Seek Command

4.5.5 Format Command

For a Format command (CSR bits 3-1, Op Code 000), the DAR contains three separate information fields as shown in Figure 4-6. Table 4-4 gives the DAR bit definitions during a format command. Bit 15 represents the command modifier field and specifies the performance of one of two different functions. The remaining two fields each specify parameters related to the execution of the Format Disk command modifier.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mdfr.	Maxumum Head				Maximum Cylinder										

Figure 4-6. DAR During Format Command

Table 4-4. DAR Bit Definitions During Format Command

Bit(s)	Function	Description
Bit 15	Command Modifier Field	Action by the ACB-SCSI upon receipt of a Format command varies depending upon the decode of these bits. See Table 4-5.
Bits 14-11	Maximum Head	This field, used only for the Format Disk command modifier, specifies the number of data surfaces on the drive, minus one.
Bits 10-0	Maximum Cylinder	This field, used only for the Format Disk command modifier, specifies the number of cylinders on the drive, minus one.

Table 4-5. Format Command Modifier Field in the DAR

Bit 15	Meaning
0	Format Disk
1	Read Parameter Defect List

A drive is formatted in one operation by placing the format parameters for the addressed drive in the fields of the DAR before writing the command to the CSR. A successful format should have a value of 0 in the CSR on completion. After a successful format, the system should be reset to allow correct power-up recognition of the drive.

4.5.6 Read Parameter and Defect Lists

This command reads the parameter list provided to the SCSI target controller at the time the disk was formatted. The list contains four sections, the first three of which conform precisely to the SCSI specified format for Mode Select Parameter, Extent Descriptor, and Drive Parameter lists respectively. The fourth section specifies the total number of data blocks available to the host. The list, 26 bytes in length, is placed in host memory starting at location 1000H. Specific byte format, in terms of host memory addresses, is shown in Table 4-6.

The command also reads the defect list for the addressed target. It is then appended in host memory to the last parameter list. The list conforms to the SCSI specified format. The length of the defect list is variable

Byte format in terms of host memory addresses is shown in Table 4-7.

Table 4-6. Parameter List Format

Address(H)	Function	Code(H)	F/V (Fixed/Variable)
1000-1002	Reserved	00 00 00	F
1003	Extent Descriptor Length	08	F
1004	Density Code	00	F
1005-1008	Reserved	00 00 00 00	F
1009-100B	Block Size	00 20 00	V (512 bytes)
100C	List Format Code	01	F
100D-100E	Cylinder Count	01 32	V (306 cylinders)
100F	Head Count	04	V (4 heads)
1010-1011	Reduce Write Current Cyl.	01 00	V (Cylinders 256)
1012-1013	Write Pre-Compensation Cyl.	01 00	V (Cylinders 256)
1014	Landing Zone Position	08	V
1015	Step Pulse Rate	01	V
1016-1017	Number of Blocks	51 46	V (21830)

Table 4-7. Parameter and Defect List Format

Address(H)	Field Definition	Code(H)	F/V (Fixed/Variable)
101A-101B	Reserved	00 00	F
101C-101D	Defect List Length	xx xx	V (8n+4)
101E-1020	Cylinder Number	xx xx xx	V (Definition 1)
1021	Head Number	xx	V (Definition 1)
1022-1025	Byte Offset *	xx xx xx xx	V (Definition 1)

* From index

Format from 101F to 1025 is repeated "n" times.

4.6 Sense Word Registers (SWR0, SWR1, SWR2)

The Sense Word Registers hold information about commands that terminate due to an error.

4.6.1 Sense Word Register 0

The ACB-SCSI loads Sense Word Register 0 (SWR0) in the event of either of two abnormal occurrences:

1. A sequence control error (CSR bit 12) within the ACB-SCSI was detected.
2. An error was detected by the target controller. The occurrence of this type of error is signalled to the ACB-SCSI by means of a premature SCSI status phase accompanied by the *check* bit set in the completion status returned by the target controller. This event is initially indicated to the host processor by setting CSR bit 11.

Table 4-8 gives the bit definitions for SWR0.

Table 4-8. Sense Word 0 Register Bit Definitions

Bit(s)	Function	Description
Bits 15-8	SCSI Command Op Code	This field indicates the op code for the SCSI command being executed at the time of the error. Specific op codes and their meanings are defined in Table 4-6.
Bits 7-0	ACB-SCSI Completion Code	This field contains errors detected by the ACB-SCSI, the result of which was the setting of CSR bit 12 and premature termination of the operation in progress as defined in the SCSI command op code field of this sense word. See Table 4-9.

Table 4-9. ACB-SCSI Completion Codes

Code	Error
00	No Errors
01	Interrupt Error (SPC)
02	Adapter Control Check
04	Phase Change Error
08	Selection Error
10	Self Test Error (SPC)
20	Bad Media (Too Many Defects)

4.6.2 Sense Word Register 1

The ACB-SCSI loads Sense Word Registers 1 and 2 when an error is detected by the target controller. Figure 4-7 shows the SWR1 format. Table 4-10 gives the bit definitions for this register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A V	Error Class			Error Code				Reserved			Logical Block Address (MSB)				

Figure 4-7. Sense Word Register 1 Format

Table 4-10. SWR1 Bit Definitions

Bit	Function	Description
Bit 15	Address Valid	This bit indicates that the logical block address field contains valid information.
Bits 14-12	Error Class	The two following fields indicate the failure in terms of an error class and an error code. This field expresses the error in terms of one of three possible classes. 1. Class 0: Drive Errors 2. Class 1: Target Controller Errors 3. Class 2: System Related Errors
Bits 11-8	Error Code	This field indicates a code which defines the specific failure. Refer to Tables 4-11, 4-12 and 4-13 for Class 0, 1, and 2 error codes.
Bits 7-5		Reserved
Bits 4-0	Logical Block Address	Most significant byte

Table 4-11. Class 0 Error Codes

Code	Error
00	No Sense
01	No Index Signal
02	No Seek Complete
03	Write Fault
04	Drive Not Ready
06	No Track 00

Table 4-12. Class 1 Error Codes

Code	Error
10	ID CRC Error
11	Uncorrectable Data Error
12	ID Address Mark Not Found
13	Data Address Mark Not Found
14	Record Not Found
15	Seek Error
16-17	Not Assigned
18	Data Check In No Retry Mode
19	ECC Error During Verify
1A	Interleave Error
1B	Not Assigned
1C	Unformatted Or Bad Format On Drive
1D	Self Test Failed
1E	Too Many Bad Blocks
1F	Not Assigned

Table 4-13. Class 2 Error Codes

Code	Error
20	Invalid Command
21	Illegal Block Address
22	Not Assigned
23	Volume Overflow
24	Bad Argument
25	Invalid Logical Unit (Device) Number
26-2F	Not Assigned

4.6.3 Sense Word Register 2

Sense Word Register 2 contains the remaining two bytes of the target device logical block address. Figure 4-8 illustrates the SWR2 format.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Logical Block Address								Logical Block Address (LSB)							

Figure 4-8. Sense Word Register 2 Format

BLANK

SECTION 5: SCSI/U SOFTWARE INTERFACE

This section describes the software interface between a host and the SCSI/U host adapter. After initialization, the SCSI/U board communicates with the host through buffers in host memory. Some buffers are used primarily for initializing and controlling the communication channel between the host and SCSI/U; others contain command packets that the host has written to memory or status packets that the SCSI/U has returned to memory. A "packet" is a structured set of fields that the host writes and the SCSI/U reads, interprets, and acts upon if requested to do so. The SCSI/U returns the status fields of a packet to memory when its task is finished.

After a brief description of the initialization process, the structure of packets and definitions of packet fields will be the subject of the rest of this section.

5.1 Initialization

Initialization occurs in two stages on the SCSI/U. The first stage is completed after a power up and self-diagnostic cycle. The second stage is completed only after the SCSI/U has obtained addresses of control registers and message buffers in host memory. From control registers in host memory, the SCSI/U knows when the host has a command for a target on the SCSI bus. The buffers contain specific command data and an address where the SCSI/U will return completion status.

5.1.1 First Initialization Phase

At power up, the SCSI/U automatically returns $FFFF_H$ (auto reply) when the host attempts to access regport— the VMEbus base address for the SCSI/U board. The SCSI/U then begins self-diagnostics. The SCSI/U generates an auto reply whenever it is accessed while busy, as it would be while diagnostics check the SCSI Protocol Controller (SPC) and RAM.

Diagnostics: An LED on the SCSI/U board signals the start of diagnostics with one long and one short blink. It signals the end of diagnostics with one long and two short blinks. If the diagnostics fail, auto reply remains enabled, the SCSI/U in effect ignores the host until the fault is corrected, and the LED blinks an error code, the interpretation of which is presented in Table 5-1.

Table 5-1. Power Up Diagnostics

LED	Interpretation
One long blink	SPC diagnostics failed
Two long blinks	RAM test failed
Three long blinks	SPC interrupt failed to occur
Four long blinks	SPC did not post its function complete
Five long blinks	No SPC data full bit received
Six long blinks	Register data did not compare

After diagnostics are completed the LED goes on only when the microprocessor is waiting for an interrupt from the SCSI bus, or when it is monitoring access port. The diagnostic LED is out while the SCSI/U actively responds to a command.

If the diagnostics are successful, the SCSI/U turns auto reply off and begins monitoring access port for a host access.

If the host attempts to read the SCSI/U at this point, the SCSI/U returns IDENT $(72XX)_H$. The three low order bits of IDENT encode the SCSI/U ID on the SCSI bus. More than one SCSI/U board can reside on a single SCSI bus: the ID allows a host to distinguish between them. The address is jumper selectable from the values 0-7. A single SCSI/U is normally set at the default level 07. The remaining bits (3-7) in the low

order byte of IDENT are defined in Table 5-2.

During the first phase of initialization, the SCSI/U also reads the setting of on-board parity jumpers to determine whether parity is enabled or disabled.

5.1.2 Hard Initialization Phase

The first phase of initialization is finished when the SCSI/U has completed diagnostics and turned auto reply off. Before any other commands are written to the SCSI/U, the host must provide it with the address of a control register and packet buffers in memory that will be used for all further communication. The protocol for a hard initialization consists of a sequence of commands and returns between the host and SCSI/U adapter. The host initiates the protocol by sending a hard initialization command ($F1XX_H$) to the SCSI/U. The host sets bit 4 in the low order byte of this command if the SCSI/U must reset the SCSI bus during hard initialization. Bit 5 is set if the SCSI/U is to ignore the host response timeout. Bits 0-3 and 6-7 in the low order byte are reserved.

After the SCSI/U reads the $F1XX_H$ command it returns the one's complement of the command back to the host. After receiving the compliment, the host must immediately write three words in succession to r0. The high byte of the first word contains the Bus Width (BW) that will be used to load the Host Adapter Control Block (HACB). The next two words are the 32 bit address of the HACB, where the SCSI/U obtains its commands. If r0 is read any time after the SCSI/U reads the last of the three words, and auto reply is off, it returns $72XX_H$ (ident) which lets the host know that the initialization was completed successfully.

5.2 Summary of SCSI/U Returns

Communication between the host and SCSI/U begins when the host accesses regport (r0) over the VMEbus, and the SCSI/U generates a return. Depending on the status of the SCSI/U and the setting of the read/write bit in access port, the SCSI/U will return one of the following:

Table 5-2. SCSI/U Initialization Returns

VMEbus Signal	SCSI/U Return	Interpretation
DTACK*	$FFFF_H$	Automatically generated in response to a read when auto reply is on and the SCSI/U is accessed but is busy, as it would be during initialization.
DTACK*	$72XX_H$(ident)	Generated when an attempt is made to read the SCSI/U, if the SCSI/U is not busy, and auto reply is off. The XX bits 0-7 in the IDENT return are interpreted as follows: Bit 7 Bit 7 set to 0, this bit indicates SCSI/U. Bit 7 set to 1 is unassigned. Bit 6 Set when parity is enabled. Bit 5 Set when the SCSI/U is initialized. Bit 3-4 Reserved. Bit 0-2 Returns the SCSI/U ID, a value of 0-7 that is the address of the SCSI/U on theSCSI bus.
BERR*		When auto reply is off this VMEbus signal is returned if the host attempts to address any register other than r0 on the SCSI/U. It is also returned if the exact steps of an initialization are not followed.
DTACK*	Complement	The one's complement of the hard initialize command is returned to the host any time after the first phase of initialization, if the host writes a hard initialize ($1FXX_H$) followed within 100 µs by a read command, and if auto reply is off. This protocol begins the hard initialization cycle.

5.3 Host Adapter Control Block (HACB)

The HACB is a four word memory location on the host CPU. It is shown as the first four words in Figure 5-1. The first word in the HACB is the Device Control Register (DCR) which contains eight GO bits in its MSByte. Each of these bits corresponds to one of the eight possible devices on the SCSI/U bus. The SCSI/U itself is GOx, where "x" is the address of the SCSI/U on the SCSI bus. If a GO bit is set, the SCSI/U obtains a command packet for the corresponding device from host memory and begins executing the command. The LSByte in the DCR contains eight Device Busy (DB) bits that the SCSI/U sets before executing the command that was initiated by a GO bit. After completing a job, the SCSI/U resets the GO bit, but leaves the DB set, so the host will know that its command has been completed.

If a GO bit is set in the DCR with no corresponding DB bit, the SCSI/U knows it has a new job from the host. If a DB bit is set with no corresponding GO bit, the host knows that the SCSI/U has completed a job. If corresponding bits are set, the host knows that the SCSI/U is working on a particular job. The DCR thus indicates when commands are pending for the SCSI/U, when the SCSI/U is busy, and whether or not the SCSI/U has completed a requested command.

The second and third words of the HACB are the Host Arbitration Register (HAR) and the Controller Arbitration Register (CAR). These registers are essentially semaphores that are set either by the host or SCSI/U when one or the other wants to read, write, or modify the DCR. As long as either the host or SCSI/U has set a bit in its arbitration register, the other can not perform any action on the DCR until the first is through. The registers are provided only for installations without a true read, modify, write sequence.

The fourth word in the HACB is reserved, as shown in Figure 5-1.

5.4 SCSI Control Block (SCB)

The SCSI Control Block (SCB) is contiguous with the HACB. It consists of eight consecutive Device Control Blocks (DCB). Each DCB is 16 words long with an eight word block identified as the SCSI Communication Control Block (CCB) and an eight word long Command Descriptor Block (CDB). The SCB is shown in Figure 5-1 as words 4-11.

	Bit # 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word 0	GO7	GO6	GO5	GO4	GO3	GO2	GO1	GO0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Word 1	Host Arbitration Register															
Word 2	Controller Arbitration Register															
Word 3	Reserved															
Word 4	Device Control Block 0															
Word 5	Device Control Block 1															
Word 6	Device Control Block 2															
Word 7	Device Control Block 3															
Word 8	Device Control Block 4															
Word 9	Device Control Block 5															
Word 10	Device Control Block 6															
Word 11	Device Control Block 7															

Figure 5-1. HACB and SCB Registers

After the SCSI/U knows the VME address of the HACB, it arbitrates for the VMEbus every 100 µs if there is a job in progress, every 1 Ms if there is not, to examine the GO bits in the DCR. If a bit is set, the SCSI/U obtains the appropriate DCB from the SCB and begins to execute the instructions it contains. The structure of the DCB is presented in Figure 5-2.

	Bit # 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word 0	ERR	Reserved			CERR				SCSI STATUS							
1	IE	DIR	SW	DISC	Reserved				CDBLEN							
2	BW		AM						IV							
3	DADR (MSB)								DADR							
4	DADR								DADR (LSB)							
5	DLEN (MSB)								DLEN							
6	DLEN								DLEN (LSB)							
6	DBSZ (MS)B								DBSZ (LSB)							
8	SCSI Command Code (CMD)								LUN			Defined by Command				
9	Defined by Command types 0, 1, & 7								Defined by Command types 0, 1, & 7							
10	Defined by Command types 0, 1, & 7								Defined by Command types 0, 1, & 7							
11	Defined by Command types 1 & 7								Defined by Command types 1 & 7							
12	Defined by Command types 1 & 7								Defined by Command types 1 & 7							
13	Defined by Command type 7								Defined by Command type 7							
14	Defined by Command type 7								Defined by Command type 7							
15	Defined by Command type 7								Defined by Command type 7							

Figure 5-2. Device Control Block Structure

The CDB, consisting of words 8-15 in the DCB, is identical to the CDB described by ANSI SCSI Standard 39.131-1986. A type 0 command is six bytes long, so the last five words are ignored. A type 1 command is ten bytes long, so the last three words are ignored. A type 7 command is vendor unique and may be as long as eight words.

5.5 Command Execution

Immediately after reading the three words in the hard initialization protocol, the SCSI/U crosses the VMEbus and looks for GO bits in the DCR. So, if the host wants the SCSI/U to respond to a target command immediately after a hard initialize, it must set a GO bit before issuing the initialize command. When the SCSI/U finds a GO bit, it sets the corresponding DB bit, fetches the DCB for the selected target, reads the appropriate fields in the DCB and the CDB and starts command execution. The DCB fields and their interpretations are listed below.

LUN — The host selects one unit on a target in the Logical Unit Number field. After the SCSI/U reads this field, it sends the selected unit on the target an IDENTIFY message to open a data transfer channel on the bus.

CDBLEN — The Command Descriptor Block Length tells the SCSI/U how many bytes in the command itself are valid, so it sends that many bytes to the target.

CMD — The SCSI/U only reads the command field if the command is directed to it, rather than to one of the seven other targets. It does not pay attention to specific commands directed to a target. Not all commands in this field will request the transfer of data. If a request is made, however, the SCSI/U interprets the following DCB fields.

DIR — If the DIRection bit is set, the data direction is from the host to the target. If the DIR is cleared, the direction is reversed.

SW — If the SWap bit is set, the SCSI/U will swap bytes in each word of data transferred to and from the SCSI target.

DISC — If set to 1, disconnects are disabled.

DADR — The SCSI/U receives data from or sends data to the address specified by the 32 bit wide pointer in the Data ADDRess field.

BW	The Bus Width is reserved for future use. Currently set at a word wide data transfer.
IE	The Interrupt Enable bit is set when the host directs the SCSI/U to interrupt it after a command is completed. If this bit is not set, the SCSI/U still resets the GO bit in the DCR to zero when the command is completed, but does not generate an interrupt.
AM	The Address Modifier field is reserved for future use.
IV	The Interrupt Vector field is reserved for future use.
DLEN	If the 32 bit data length field of the DCB contains a byte count, and the data block size field is specified, the SCSI/U determines whether padding is required to make the transfer an even multiple of the specified block size. If so, the padding is added.
DBSZ	The size of each data block is specified in this 16 bit field.

Except for its own host adapter commands, the SCSI/U passes all commands directly to the appropriate target and tracks commands that require transfers until they are competed by allowing the target to disconnect and reselect as until the transfer is complete. After the last data is transferred, the SCSI/U returns status to the host. The status is returned in the zero word of the DCB, which consists of the following fields:

ERR	Bit 15 is reserved for a system error flag (ERR) to inform the host an error has occurred. This bit is set whenever CERR or the STATUS byte are non-zero.
CERR	The Controller Error (CERR) bits are reserved for the SCSI/U controller. Error codes are summarized in Table 5.2.
STATUS	The STATUS byte returns status from the selected target, which are standard SCSI status returns. For convenience, the standard SCSI status returns are listed in Table 5.3.

After the SCSI/U has completed a command and returned any error and status codes, it clears the GO bit associated with the command, but leaves the DB bit set, so the host will know that the particular command is completed. For convenience, the ANSI standard status codes are presented in Table 5-3.

Table 5-3. STATUS Codes

Code	Interpretation
00_H	Good Status
02_H	Check Condition
04_H	Condition Good
08_H	Device Busy
10_H	Intermediate: Linked/Good Status
12_H	Intermediate: Linked Condition
18_H	Reservation Conflict

Table 5-4. CERR Codes

Code	Interpretation
00_H	No error.
01_H	An error was detected in the command from the host.
02_H	The target failed to respond to a select command within approximately 250 µs.
03_H	The SPC failed to time out during select.
04_H	An anticipated interrupt arrived, but was of the wrong type, such as a disconnect interrupt from an unconnected target.
05_H	The firmware timed out waiting for a target to respond to a phase change; this error occurs while waiting for a bus service interrupt.
06_H	Phase control error: a bus service interrupt is directing the wrong sequence.
07_H	The VMEbus address was bad, either because it was not right in the DCB, or the SCSI/U miscalculated.
08_H	The target failed to return status.
09_H	A target that was connected or not active requested a reconnect.
$0A_H$	The data direction requested by the SPC does not match the direction requested by the host.
$0B_H$	The target disconnected without warning, that is, without sending a completion or status notice.
$0C_H$	A forced disconnect (Reset) was sent to the target because it did not relinquish the SCSI/U bus after a reasonable (>1 sec) interval. All other targets forced off the bus will return $0D_H$ in response to this reset. The target that hung on the bus will return $0C_H$.
$0D_H$	This code is returned by all targets that were forced off the SCSI bus due to a forced reset, except for the hung target, as explained above.
$7FOA_H$	This code indicates any CERR or STATUS system level error.

5.6 SCSI/U Commands

Commands initiated by setting GOx in the DCR (where "x" is the jumper selected SCSI bus address of the SCSI/U) are meant for the SCSI/U board itself, rather than one of the other 7 targets on the SCSI bus. These commands are defined by ISI, and other commands to the board are illegal and will be rejected. Private commands are written in the high byte of the CDB, as are all other target commands. If data is sent or returned, the data address, length and block size fields are used. The command initiated by setting GOx in the DCR is completed when the SCSI/U resets GOx, but leaves the corresponding DBx bit set. The STATUS byte and CERR bits are returned.

VME-SCSI/U Commands

Reset $F0_H$ — Resets the SCSI/U board and SCSI bus. No data is transferred. The data length field must be zero bytes; the DIR flag is ignored.

Init $F1_H$ — This is similar to the hard initialize command that is sent to register 0 when auto reply is off, except that this command does not wait until the SCSI/U is not busy. It does require that the SCSI/U has previously completed hard initialization. The firmware accepts three words of data from the address presented in the data address field of the DCB and uses them for the address of a new HACB, a new AM, and a new BW. Other fields in the DCB that must be set include the 4 byte data length field, the 1 byte DBSZ field, and the DIR flag, which is set to send. The new HACB takes effect when the GO bit is cleared in the DCR,

and (optionally) the SCSI/U interrupts the host. All pending operations are aborted by the controller when it receives this command.

Status $F2_H$ This debugging command may not be supported on all versions. The length and format of returned data is subject to change without notice, depending on the version of firmware used on any given board. The data that the SCSI/U returns status varies in length, depending on the data length requested by the host. The first word always consists of controller flags. The next eight words indicate the current status and command progression of all devices on the SCSI bus. Data length for this command is xx bytes, depending on the host request. Data block size is one byte. The DIR flag must be set to receive.

Version $F3_H$ Upon receiving this command, the SCSI/U returns the version of its firmware in four data words to the address specified in the data address field of the DCB. The format is six ascii characters: GPS_XX.X. Data length in the DCB must be 8 bytes; block size is 1 byte. The DIR flag is set to receive.

DumpMem $F4_H$ This debugging command may not be supported on all versions. The length and format of returned data is subjet to change without notice, depending on the driver in the host. This command returns the controllers registers to the ISI 68KXX. The firmware returns as much state information as will fit into the specified data length. The format of the information is dependent on the firmware version of the controller. Data block size is 1 byte. The DIR flag is set to receive.

Diag $F5_H$ The SCSI/U generates a number of error messages for the target when the first byte (Byte 0) in the CDB is $F5_H$. Byte 2 in the CDB holds the id of the target that will be tested by receiving an error code. Byte 3 identifies the error that will be generated. The bits in byte 3 are interpreted as follows:

- Bit 0 Bit 0 is set to generate a message parity error. The target is told that its last message contained a parity error.
- Bit 1 Bit 1 is set to tell the target that a parity error was generated during its latest status report.
- Bit 2 Bit 2 is set to generate an error detected by the SCSI/U during a data transfer.

The fifth SCSI/U command is for diagnostic purposes only. It has no purpose other than to test the reaction of a target to an initiator generated error message.

5.7 SCSI/U States

After the SCSI/U is initialized, it is either looking for work or working. It looks for work by monitoring its access port, by looking at regport, and by crossing the VMEbus to read the DCR.

The SCSI/U can also be interrupted by the SPC, when a target requires a disconnect or reconnect, when an error occurs on a target, or when a job is finished. After receiving an interrupt, the SCSI/U services the requesting target, then reads the DCR to see if the host has attempted to select a new target. If the SCSI/U finds a new GO bit set, it services the request. If the DCR has not changed from the time the SCSI/U last accessed it, the SCSI/U returns to monitor access port. The SCSI/U continues monitoring access port and the DCR until an interrupt from the SPC requires attention, or a GO bit is set in the DCR.

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